IN THE CLAIMS

1-18. (Canceled)

19. (New) A nonvolatile semiconductor memory device, comprising:

a semiconductor substrate having a peripheral circuit region and a memory cell region;

a plurality of erasable and programmable memory cell transistors each having a gate electrode and provided in the memory cell region;

a selection transistor having a gate electrode and provided in the memory cell region;

a peripheral transistor having a gate electrode and provided in the peripheral circuit region;

first post-oxidation films each provided on the gate electrode of all of the plurality of erasable and programmable memory cell transistors;

a second post-oxidation film provided on the gate electrode of the selection transistor;

a third post-oxidation film provided on the gate electrode of the peripheral transistor; and

an insulating film covering the plurality of erasable and programmable memory cell transistors, the selection transistor and the peripheral transistor, the insulating film being harder for an oxidizing agent to pass there through than a silicon oxide film, and the insulating film having an oxidized region,

wherein the insulating film comprises a silicon nitride film, and the oxidized region is provided in a surface of the silicon nitride film.

20. (New) The device according to claim 19, wherein a thickness of the oxidized region of the silicon nitride film is not smaller than 1 nm and not larger than 10 nm.

21. (New) The device according to claim 19, wherein the silicon nitride film contains hydrogen with a concentration not larger than 3×10^{21} atom/cm^3.

22. (New) The device according to claim 19, wherein the silicon nitride film contains hydrogen, and a concentration of the hydrogen gradually becomes higher from the surface of the silicon nitride film.

23. (New) The device according to claim 19, wherein the gate electrode of each of the plurality of erasable and programmable memory cell transistors, the selection transistor, and the peripheral transistor contains a metal or a metal silicide.

24. (New) The device according to claim 23, wherein the metal contains tungsten.

25. (New) The device according to claim 19, wherein the gate electrode of each of the plurality of erasable and programmable memory cell transistors, the selection transistor, and the peripheral transistor is a stacked gate structure including a floating gate and a control gate, the control gate comprising a metal or a metal silicide.

26. (New) The device according to clam 25, wherein the metal contains tungsten.

27. (New) The device according to claim 19, further comprising:

a contact plug connected to one of a source and a drain region of the selection transistor,

wherein the memory cell transistors are series-connected to each other, one of the memory cell transistors is connected to the contact plug via the selection transistor, and the silicon nitride film covers a side wall of the gate electrode, each of the memory cell transistors, and the selection transistor.

28. (New) The device according to claim 27, wherein the silicon nitride film covers a side wall of the gate electrode of the peripheral transistor, and a thickness of a portion of the silicon nitride film covering the side wall of the gate electrode of the selection transistor and a thickness of a portion of the silicon nitride film covering the side wall of the gate electrode of the peripheral transistor are approximately the same.

29. (New) The device according to claim 27, wherein a thickness of the oxidized region formed in a portion of the silicon nitride film covering the side wall of the gate electrode of the selection transistor and a thickness of the oxidized region formed in a portion of the silicon nitride film covering the side wall of the gate electrode of the peripheral transistor are approximately the same.

30. (New) The device according to claim 27, wherein the memory cell transistors construct a NAND EEPROM.

31. (New) The device according to claim 27, wherein the memory cell transistors construct an AND EEPROM.

32. (New) A nonvolatile semiconductor memory device, comprising:

a semiconductor substrate having a peripheral circuit region and a memory cell region;

a plurality of erasable and programmable memory cell transistors each having a gate electrode and provided in the memory cell region;

a selection transistor having a gate electrode and provided in the memory cell region;

a peripheral transistor having a gate electrode and provided in the peripheral circuit region;

first post-oxidation films each provided on the gate electrode of all of the plurality of erasable and programmable memory cell transistors;

a second post-oxidation film provided on the gate electrode of the selection transistor;

a third post-oxidation film provided on the gate electrode of the peripheral transistor; and

an insulating film covering the plurality of erasable and programmable memory cell transistors, the selection transistor, and the peripheral transistor, the insulating film being harder for an oxidizing agent to pass therethrough than a silicon oxide film, and the insulating film having an oxidized region,

wherein the insulating film comprise a silicon nitride film, the silicon nitride film contains hydrogen, and a concentration of the hydrogen gradually becomes higher from the surface of the silicon nitride film.